Features

- fully assembled and tested
- on-board mode selection switch
- on-board PLL Lock and Loss of Signal LED indicators
- SMA connectors for all high-speed data inputs and outputs

General Description

The XBN2014A Rev 0 evaluation board is designed to simplify and speed-up the evaluation process of the GN2014A XFP TX Signal Conditioner with VCSEL Driver.

The block diagram of the XBN2014A Rev 0 evaluation board is shown on page 2.

An input signal is applied to the on-board device through the Equalizer Input (EQIn) SMA connectors using 50Ω coaxial cables. The on-board GN2014A chip performs conditioning of the received signal. The GN2014A also provides integrated modulation and eye shaping capability. The output data is available on the Serial Data Output (SDO) SMA connectors. The SDO output drivers are designed to directly modulate VCSELs. The SDO output amplitude can be selected between 300mVppd and1500mVppd using Swing Select (Adjust) control input. The SDO output Eye Crossing Point can be adjusted between 25% and 75% using CPAPol and CPA control inputs.

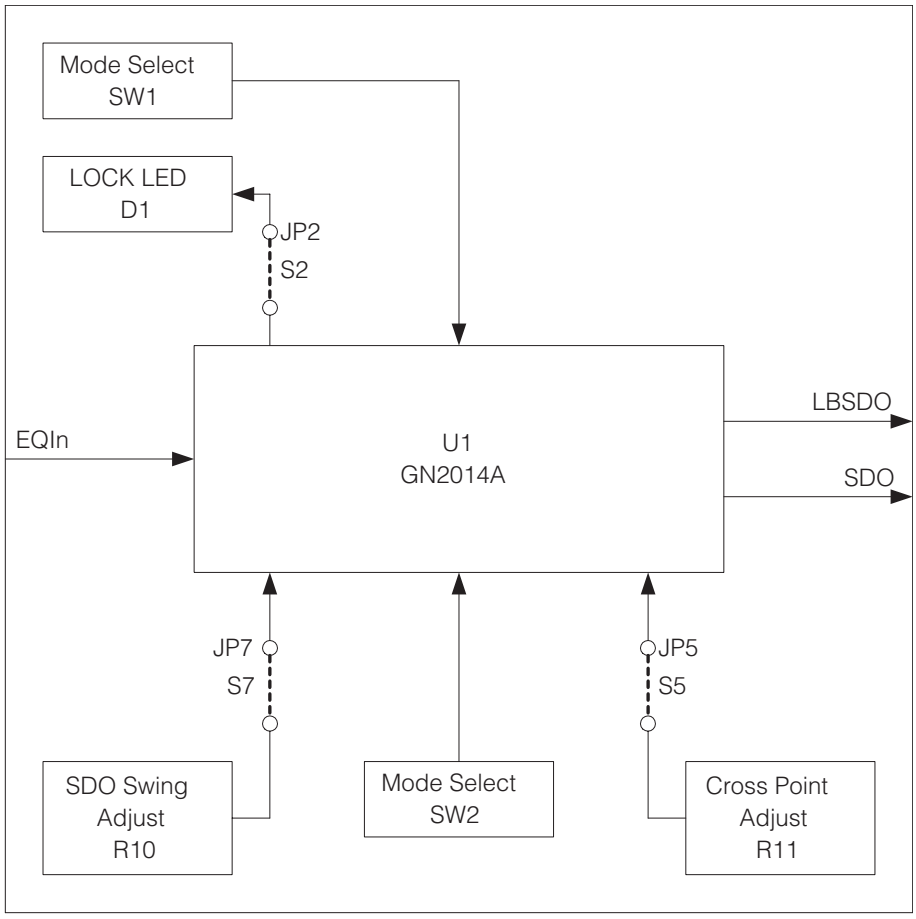
The schematic diagram of the XBN2014A Rev 0 evaluation board is shown in Figure 2-1 on page 4.

When required, the retimed data can be made available on the Loop Back Serial Data Output (LBSDO) SMA connectors. The LBSDO output can be used for interconnect troubleshooting purposes.

The PLL Lock green LED (D1), when lit, indicates the PLL's lock condition.

The PCB layout information is shown in Figure 2-2 on page 5, Figure 2-3 on page 6 and Figure 2-4 on page 7.

The XBN2014A Rev 0 printed circuit board is a four-layer, .062" board. Top layer uses RT Duriod 6002, low dielectric loss material. All other layers are standard FR-4 material. All high-speed data traces between SMA connectors and the GN2014A device are 100Ω differential microstrip lines on the top layer.



XBN2014A Rev 0 Evaluation Board Block Diagram

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1. Quick Start Sequence

1. Configure the evaluation board in accordance to the desired mode. See Figure 4-1, Figure 4-2 and Figure 4-3.
2. Connect the power supply ground to the on-board "GND" connector.
3. Connect a +3.3V power supply to the on-board "VCC" connector (current limit on the power supply should be set to 150mA).
4. Using 50Ω coaxial cables, apply an input with amplitude between 120mVppd and 1000mVppd to the EQIN SMA connectors.
5. Use the SDO SMA connectors to monitor the GN2014A data output on a high speed oscilloscope. The SDO output can also be connected to a BERT (Bit Error Rate Tester) for BER measurements.
6. Connect high-speed oscilloscope to the LBSDO SMA connectors to monitor the GN2014A LBSDO output.
7. Observe the LOCK LED.

2. Evaluation Board Schematic and PCB Layout

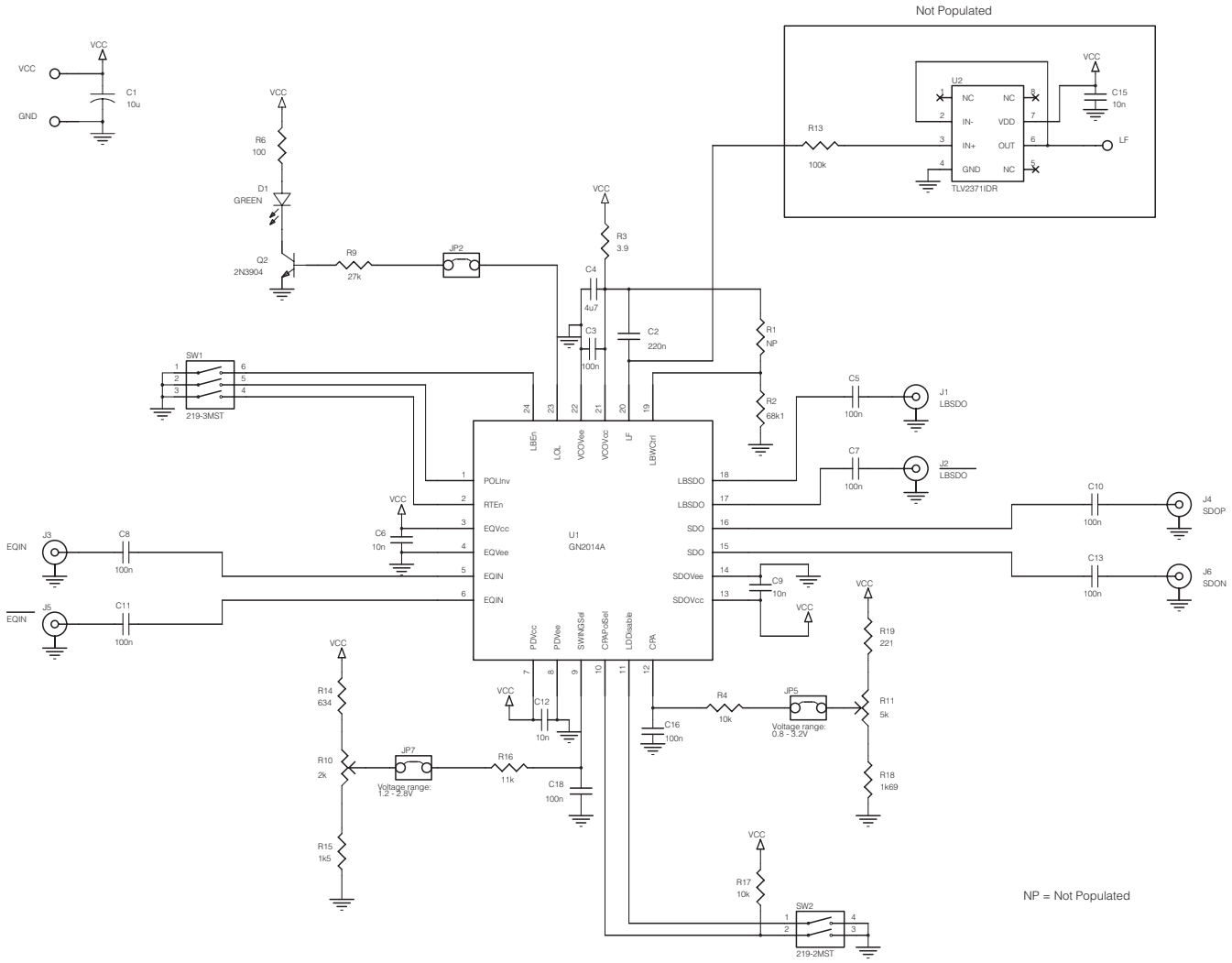


Figure 2-1: XBN2014A Rev 0 Evaluation Board Schematic

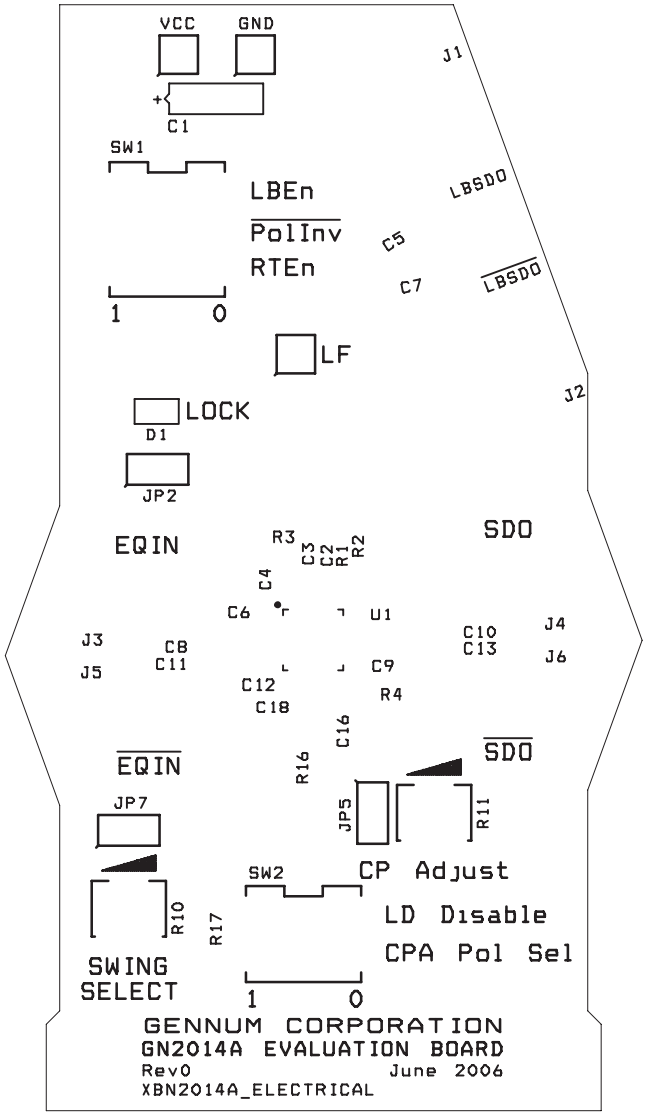


Figure 2-2: XBN2014A PCB Layout — Top Silk

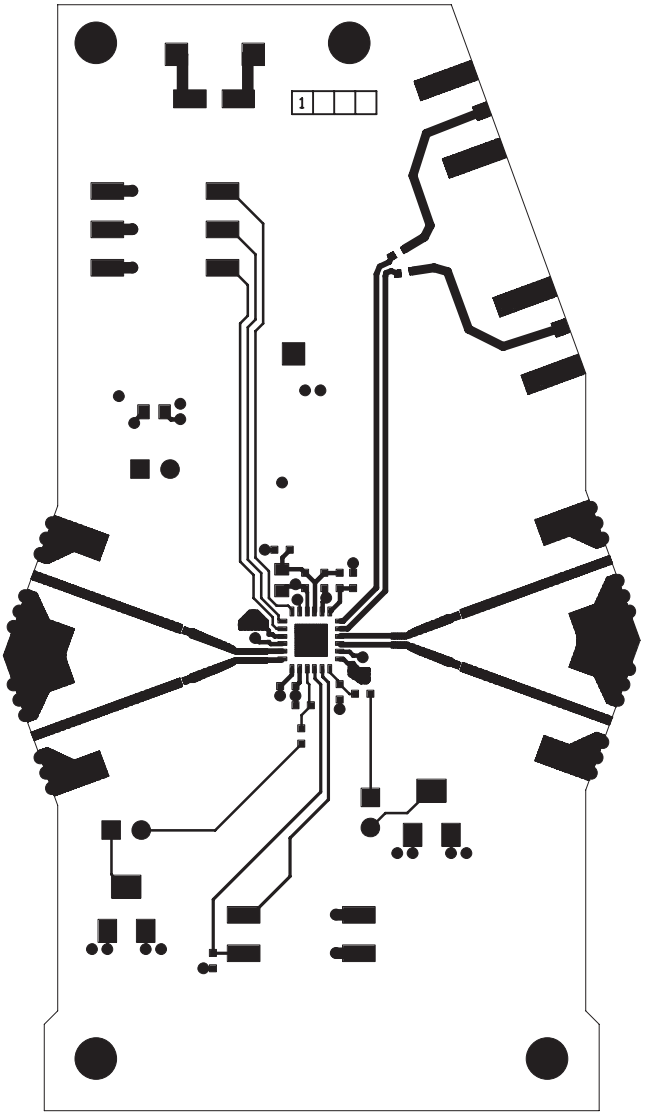


Figure 2-3: XBN2014A PCB Layout — Top Components

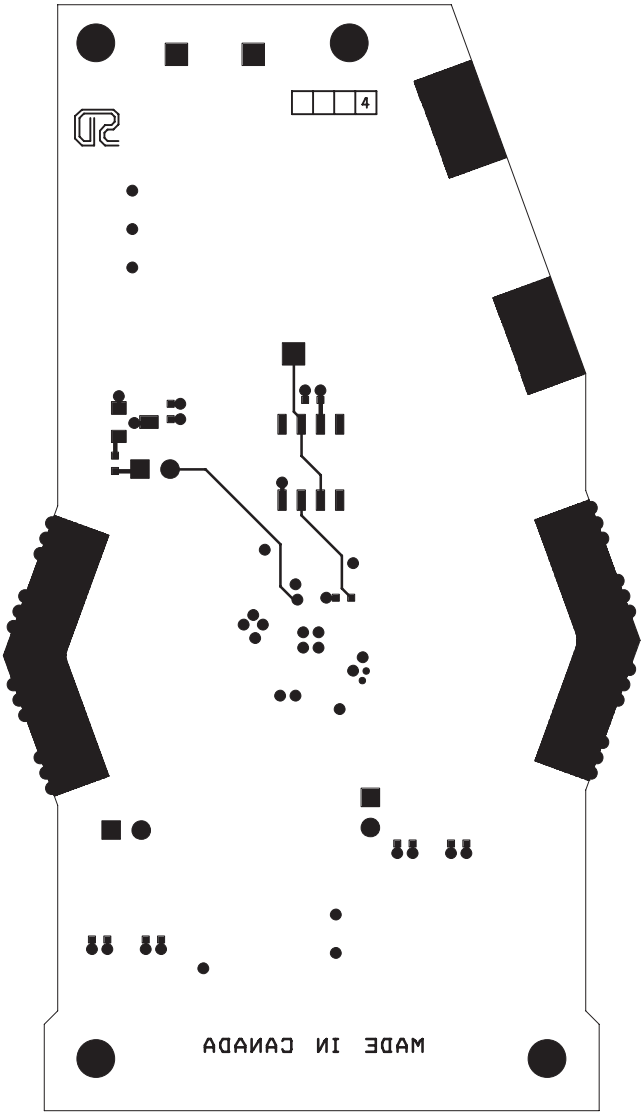


Figure 2-4: XBN2014A PCB Layout — Bottom Components

3. GN2014 Data Output Driver Swing Control

The GN2014A device is designed to directly modulate VCSELs. To accommodate VCSEL input level requirements from different manufacturers, a wide range of output amplitudes (300mVppd - 1500mVppd) can be obtained.

The GN2014A Data Output amplitude is controlled by applying 0 – 2.8Vdc control voltage to the SWNGSel control input via resistor R16 = 11kOhm.

The GN2014A evaluation board allows the Swing Select (Adjust) control voltage to be obtained in two ways:

- Using on-board potentiometer R10.

  To enable this option, place shunt S7 on JP7 jumper.

- Using external control voltage.

  To enable this option, remove shunt S7 and apply external voltage directly via JP7 jumper.

Table 3-1 shows GN2014A SDO expected amplitude for a given Swing Select (Adjust) control voltage.

Table 3-1: GN2014A Output Amplitude versus Swing Select Voltage

Swing Select Voltage at DAC (assumes 11kohm resistor in series)	GN2014A Output (Typical, LDDisable Low)	Comments
0-0.8	Soft turn on	
1.2V	150mVpp single ended	3mA modulation current
2.3V	500mVpp single ended	10mA modulation current
2.8V (Recommended Max)	750m Vpp single ended	15mA modulation current
3.3V (Reliability Max)	Not Recommended	18mA modulation max current

4. GN2014A Cross Point Adjust

The GN2014A cross point adjust is used to pre-distort the output signal to optimize optical performance. This is accompolished using two control pins:

- CPAPol (Pin 10) — Controls direction of crosspoint change, digital pin
- CPA (Pin 12) — Controls magnitude of crosspoint change, analog control

With CPA voltage set to nominal 0.8V, the output waveform will have a cross point at the 50% level, as indicated in Figure 4-1.

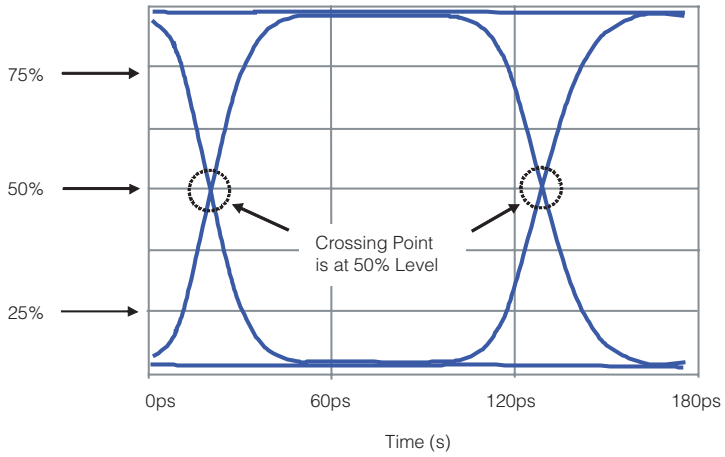


Figure 4-1: GN2014A Output Signal with CPA voltage set to 0.8V

To increase the cross point to the 75% level, the CPA polarity (pin 10:CPAPol) must be set high, and the CPA voltage (pin 12:CPA) increased to 3.1V. This results in the output waveform illustrated in Figure 4-2.

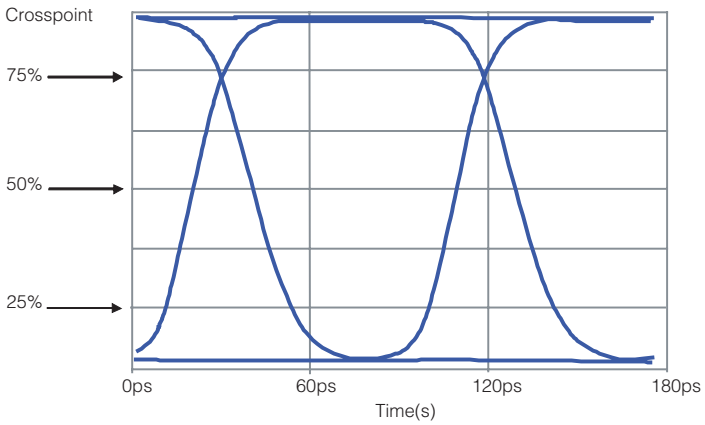


Figure 4-2: GN2014A Output Signal when CPA Polarity control input is set high, CPA = 3.1V

The cross point can be set to an intermediate level between 50% and 75% by setting the CPA to a voltage between 0.8V and 3.1V.

To decrease the cross point to the 25% level, the CPA polarity (pin 10:CPAPol) must be set low, and the CPA voltage (pin 12:CPA) increased to 3.1V. This results in the output waveform illustrated in Figure 4-3.

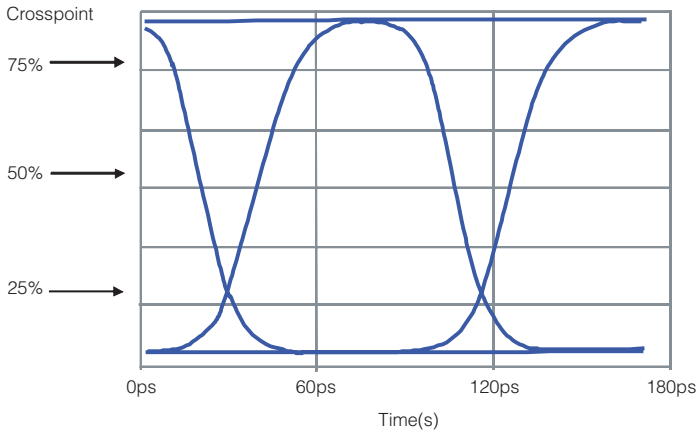


Figure 4-3: GN2014A Output Signal when CPA Polarity control input is set low, CPA = 3.1V

The cross point can be set to an intermediate level between 50% and 25% by setting the CPA to a voltage between 0.8V and 3.1V.

When these pins are left open, a 50% crosspoint is maintained.

The GN2014A evaluation board allows the Cross Point Adjust control voltage to be obtained in two ways:

- Using on-board potentiometer R11.

  To enable this option, place shunt S5 on JP5 jumper.

- Using external control voltage.

  To enable this option, remove shunt S5 and apply external voltage directly via JP5 jumper.

5. GN20014 Evaluation Board Settings

The GN2014A SONET XFP TX Signal Conditioner with VCSEL Driver can operate in various modes.

This section of the document describes the usage of SW1, SW2, JP5 and JP7 to configure some modes.

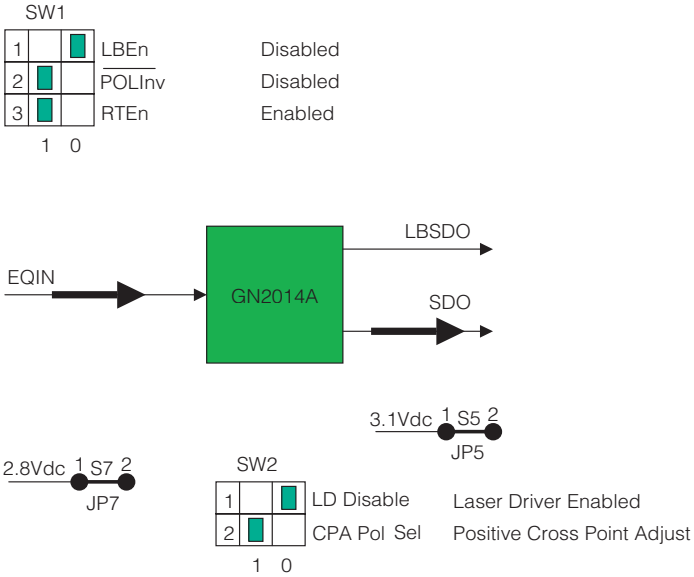
Note: Regardless of other settings, the GN2014A SDO output is muted when LD Disable control input is held "High".

5.1 Mode Configuration — Example 1

In this mode 9.95Gb/s – 11.3Gb/s data from EQIn input is first equalized and then retimed.

Configuration shown in Figure 5-1 corresponds to:

- The SDO output signal polarity: normal (not inverted), (SDOP ← LAINP and SDON ← LAINN)
- The SDO output amplitude: 1500mVppd
- The SDO Eye Cross Point: at 75%
- The retimed data is available on the SDO output only



Notes:
2.8Vdc control voltage obtained using potentiometer R10
3.1Vdc control voltage obtained using potentiometer R11

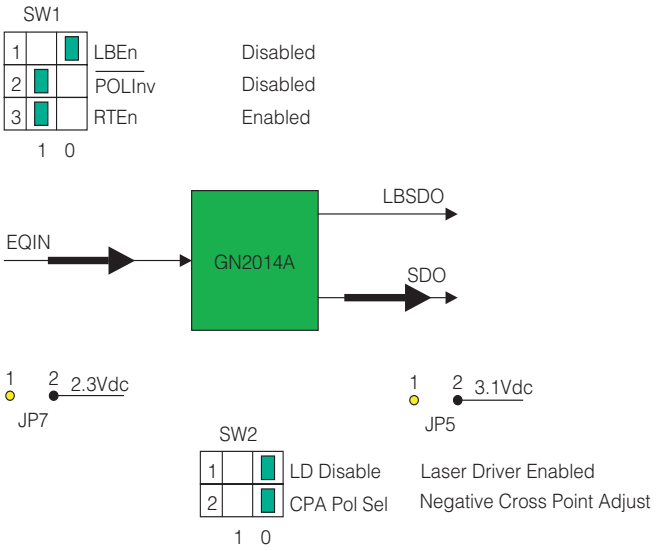
Figure 5-1: Mode Configuration — Example 1

5.2 Mode Configuration — Example 2

In this mode 9.95Gb/s – 11.3Gb/s data from EQIn input is first equalized and then retimed.

Configuration shown in Figure 5-2 corresponds to:

- The SDO output signal polarity: normal (not inverted), (SDOP ← LAINP and SDON ← LAINN)
- The SDO output amplitude: 1000mVppd
- The SDO Eye Cross Point: at 25%
- The retimed data is available on the SDO output only



Notes:
2.3Vdc control voltage obtained from external source
3.1Vdc control voltage obtained from external source

Figure 5-2: Mode Configuration — Example 2

5.3 Mode Configuration — Example 3

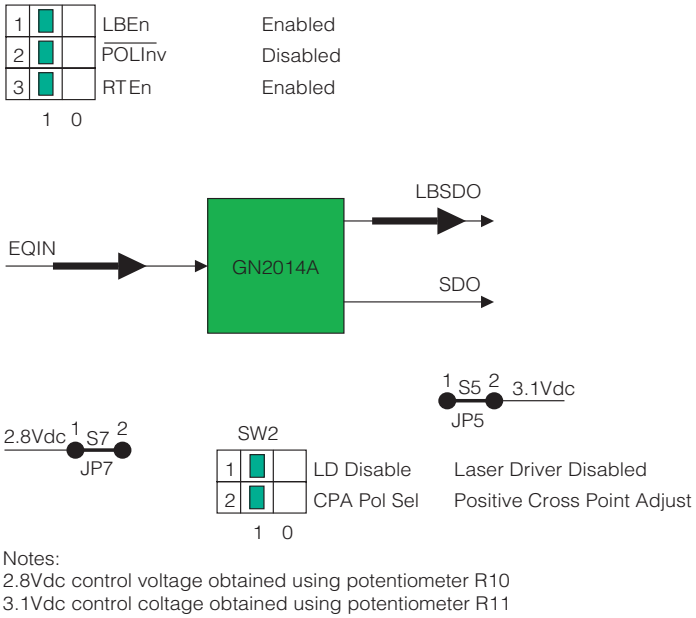
In this mode 9.95Gb/s – 11.3Gb/s data from EQIn input is first equalized and then retimed.

Configuration shown in Figure 5-3 corresponds to:

- The retimed data is available on the LBSDO output only
- The SDO output is DISABLED

Notes:

1. Laser Driver should be disabled prior enabling LoopBack SDO
2. SWNGSel and CPA settings are irrelevant for this mode, since they affect SDO output only



Notes:
2.8Vdc control voltage obtained using potentiometer R10
3.1Vdc control coltage obtained using potentiometer R11

Figure 5-3: Mode Configuration — Example 3

6. Revision History

Version	ECR	Date	Changes and / or Modifications
0	141746	August 2006	New document.

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