NTMFD4C85N

PowerPhase, Dual N-Channel SO8FL

30 V, High Side 25 A / Low Side 49 A

Features

- Co−Packaged Power Stage Solution to Minimize Board Space
- Minimized Parasitic Inductances
- Optimized Devices to Reduce Power Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- DC−DC Converters
- System Voltage Rails
- Point of Load

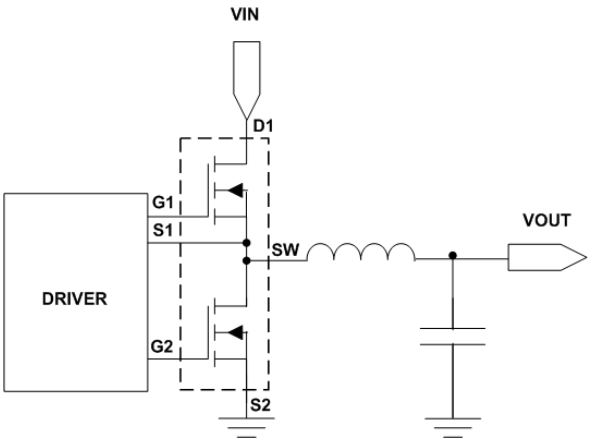


Figure 1. Typical Application Circuit

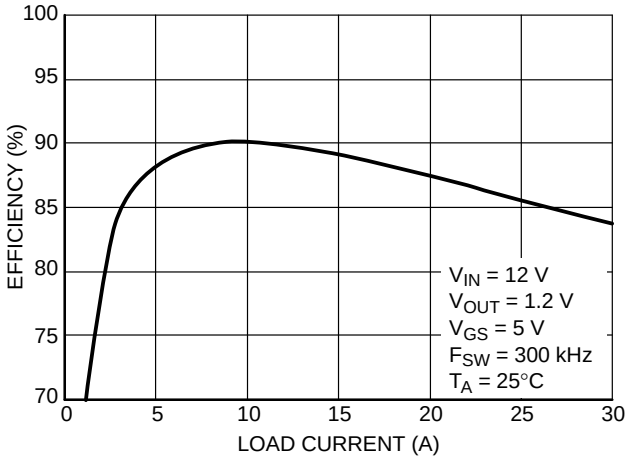
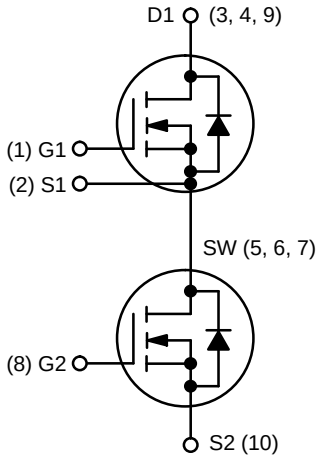


Figure 2. Typical Efficiency Performance
POWERPHASEGEVB Evaluation Board

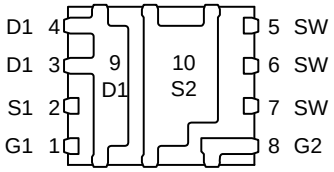
ON Semiconductor®

www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
Q1 Top FET 30 V	3.0 mΩ @ 10 V	25 A
	4.3 mΩ @ 4.5 V	
Q2 Bottom FET 30 V	0.8 mΩ @ 10 V	49 A
	1.2 mΩ @ 4.5 V	

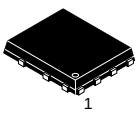


PIN CONNECTIONS

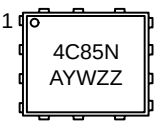


(Bottom View)

MARKING DIAGRAM



DFN8
CASE 506CR



4C85N	= Specific Device Code
A	= Assembly Location
Y	= Year
W	= Work Week
ZZ	= Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

Table 1. MAXIMUM RATINGS (TJ=25°C unless otherwise stated)

Parameter				Symbol	Value	Units
Drain−to−Source Voltage			Q1	V_{DSS}	30	V
			Q2			
Gate−to−Source Voltage			Q1	V_{GS}	±20	V
			Q2			
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	Q1	I_D	20.1	A
		T_A = 85°C			14.5	
		T_A = 25°C	Q2		39	
		T_A = 85°C			28.1	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	Q1	P_D	1.95	W
			Q2			
Continuous Drain Current $R_{\theta JA}$ ≤ 10 s (Note 1)		T_A = 25°C	Q1	I_D	25.4	A
		T_A = 85°C			18.3	
		T_A = 25°C	Q2		49.2	
		T_A = 85°C			35.5	
Power Dissipation $R_{\theta JA}$ ≤ 10 s (Note 1)		T_A = 25°C	Q1	P_D	3.10	W
			Q2			
Continuous Drain Current $R_{\theta JA}$ (Note 2)		T_A = 25°C	Q1	I_D	15.4	A
		T_A = 85°C			11.1	
		T_A = 25°C	Q2		29.7	
		T_A = 85°C			21.4	
Power Dissipation $R_{\theta JA}$ (Note 2)		T_A = 25°C	Q1	P_D	1.13	W
			Q2			
Continuous Drain Current $R_{\theta JC}$		T_C = 25°C	Q1	I_D	67	A
			Q2		174	
Power Dissipation $R_{\theta JC}$			Q1	P_D	22	W
			Q2		40	
Pulsed Drain Current		T_A = 25°C tp = 10 μs	Q1	I_{DM}	300	A
			Q2		525	
Operating Junction and Storage Temperature			Q1	T_J, T_{STG}	−55 to +150	°C
			Q2			
Source Current (Body Diode)			Q1	I_S	10	A
			Q2		10	
Drain to Source DV/DT				dV/dt	6	V/ns
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, V_{DD} = 50 V, V_{GS} = 10 V, L = 0.1 mH, R_G = 25 Ω)		I_L = 19 A_{pk}	Q1	EAS	34.5	mJ
		I_L = 26 A_{pk}	Q2	EAS	222	
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)				T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using 1 sq−in pad, 2 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size of 100 mm^2.

Table 2. THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Junction−to−Ambient – Steady State (Note 3)	$R_{\theta JA}$	64.2	°C/W
Junction−to−Ambient – Steady State (Note 4)		110.5	
Junction−to−Ambient – (t ≤ 10 s) (Note 3)		40.3	
Junction−to−Case (bottom) – Steady State Q1	$R_{\theta JC}$	5.6	°C/W
Junction−to−Case (bottom) – Steady State Q2		3.1	

3. Surface−mounted on FR4 board using 1 sq−in pad, 2 oz Cu
4. Surface−mounted on FR4 board using the minimum recommended pad size of 100 mm^2

Table 3. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	FET	Test Condition		Min	Typ	Max	Units
OFF CHARACTERISTICS								
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	Q1	V_{GS} = 0 V, I_D = 250 μA		30			V
		Q2			30			
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}$ / T_J	Q1				19		mV/°C
		Q2				17		
Zero Gate Voltage Drain Current	I_{DSS}	Q1	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1	μA
				T_J = 125°C			10	
		Q2		T_J = 25°C			1	
Gate−to−Source Leakage Current	I_{GSS}	Q1	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
		Q2					100	
ON CHARACTERISTICS (Note 5)								
Gate Threshold Voltage	$V_{GS(TH)}$	Q1	V_{GS} = V_{DS}, I_D = 250 μA		1.3		2.1	V
		Q2			1.3		2.1	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}$ / T_J	Q1				4.3		mV/°C
		Q2				4.6		
Drain−to−Source On Resistance	$R_{DS(on)}$	Q1	V_{GS} = 10 V	I_D = 20 A		2.2	3.0	mΩ
			V_{GS} = 4.5 V	I_D = 20 A		3.3	4.3	
		Q2	V_{GS} = 10 V	I_D = 30 A		0.6	0.8	
			V_{GS} = 4.5 V	I_D = 30 A		0.95	1.2	
CAPACITANCES								
Input Capacitance	C_{ISS}	Q1	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 15 V			1960		pF
		Q2				6660		
Output Capacitance	C_{OSS}	Q1				1230		
		Q2				3660		
Reverse Capacitance	C_{RSS}	Q1				102		
		Q2				126		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
6. Switching characteristics are independent of operating junction temperatures

Table 3. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	FET	Test Condition		Min	Typ	Max	Units
CHARGES & GATE RESISTANCE								
Total Gate Charge	$Q_{G(TOT)}$	Q1	V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 20 A			15		nC
		Q2				45.2		
Threshold Gate Charge	$Q_{G(TH)}$	Q1				1.5		
		Q2				4.5		
Gate−to−Source Charge	Q_{GS}	Q1				5.0		
		Q2				15		
Gate−to−Drain Charge	Q_{GD}	Q1				5.2		
		Q2				11.8		
Total Gate Charge	$Q_{G(TOT)}$	Q1	V_{GS} = 10 V, V_{DS} = 15 V; I_D = 20 A			32		nC
		Q2				99.3		
Gate Resistance	R_G	Q1	T_A = 25°C			1.0		Ω
		Q2				1.0		
SWITCHING CHARACTERISTICS (Note 6)								
Turn−On Delay Time	$t_{d(ON)}$	Q1	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 20 A, R_G = 3.0 Ω			10.3		ns
		Q2				19.5		
Rise Time	t_r	Q1				37		
		Q2				27		
Turn−Off Delay Time	$t_{d(OFF)}$	Q1				20		
		Q2				47		
Fall Time	t_f	Q1				5.6		
		Q2				15		
SWITCHING CHARACTERISTICS (Note 6)								
Turn−On Delay Time	$t_{d(ON)}$	Q1	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 20 A, R_G = 3.0 Ω			8.0		ns
		Q2				12.6		
Rise Time	t_r	Q1				31.5		
		Q2				22.7		
Turn−Off Delay Time	$t_{d(OFF)}$	Q1				25		
		Q2				60		
Fall Time	t_f	Q1				4.0		
		Q2				12.2		
DRAIN−SOURCE DIODE CHARACTERISTICS								
Forward Voltage	V_{SD}	Q1	V_{GS} = 0 V, I_S = 10 A	T_J = 25°C		0.78		V
				T_J = 125°C		0.62		
		Q2	V_{GS} = 0 V, I_S = 10 A	T_J = 25°C		0.75		
				T_J = 125°C		0.55		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
6. Switching characteristics are independent of operating junction temperatures

Table 3. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	FET	Test Condition	Min	Typ	Max	Units
DRAIN−SOURCE DIODE CHARACTERISTICS							
Reverse Recovery Time	t_{RR}	Q1	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 2 A		40		ns
		Q2			73		
Charge Time	ta	Q1			20		
		Q2			40		
Discharge Time	tb	Q1			20		
		Q2			33		
Reverse Recovery Charge	Q_{RR}	Q1			37		nC
		Q2			137		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
6. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS − Q1

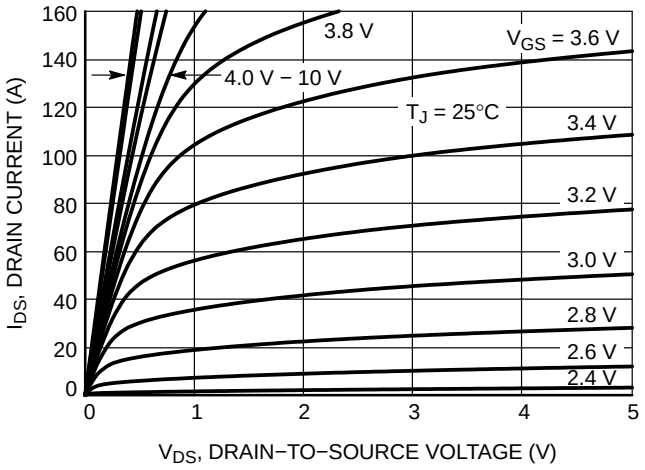


Figure 3. On−Region Characteristics

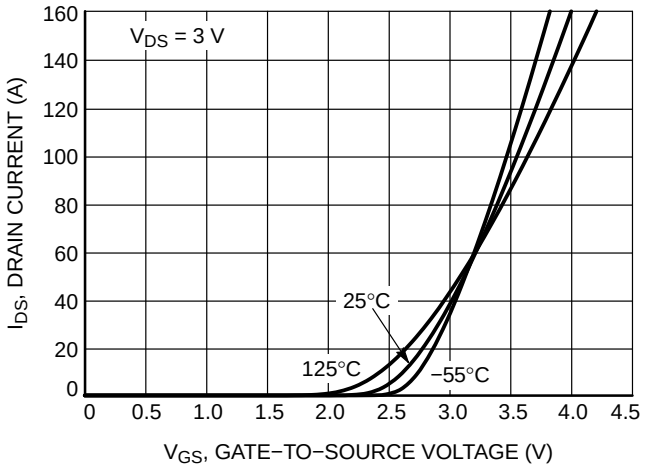


Figure 4. Transfer Characteristics

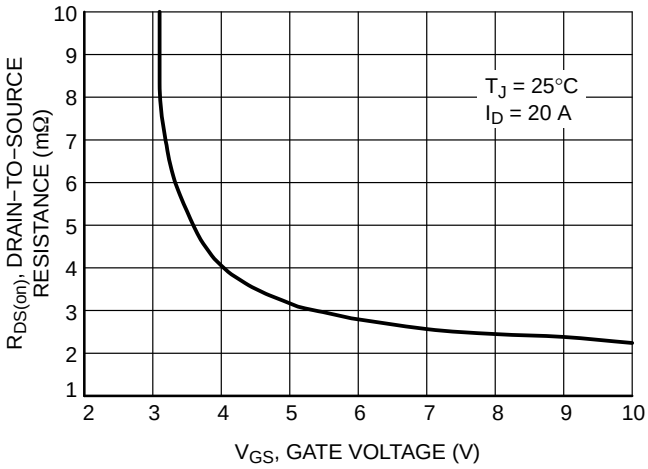


Figure 5. On−Resistance vs. Gate−to−Source Voltage

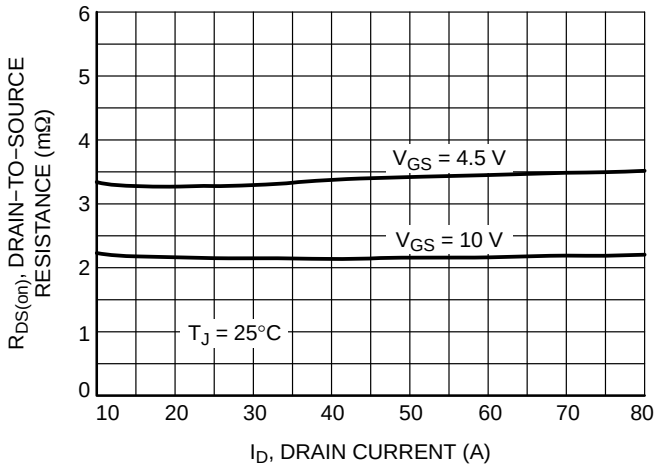


Figure 6. On−Resistance vs. Drain Current and Gate Voltage

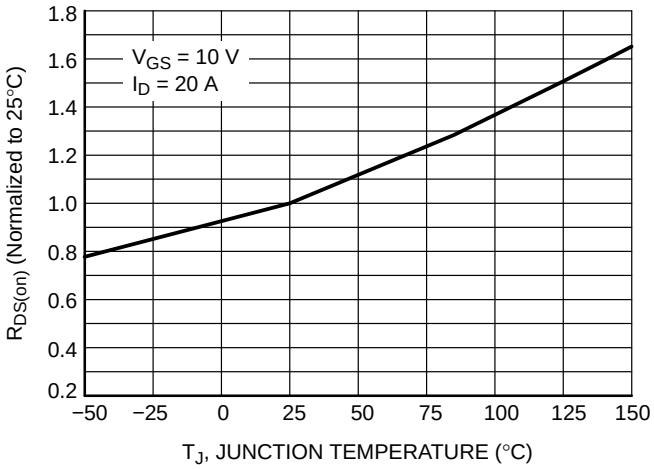


Figure 7. On−Resistance Variation with Temperature

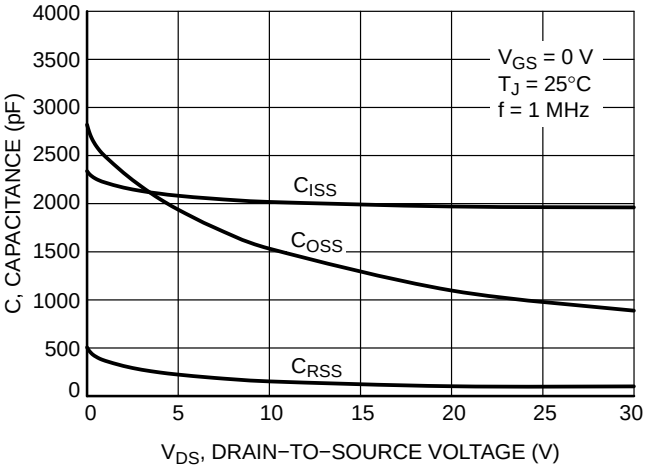


Figure 8. Capacitance Variation

TYPICAL CHARACTERISTICS − Q1

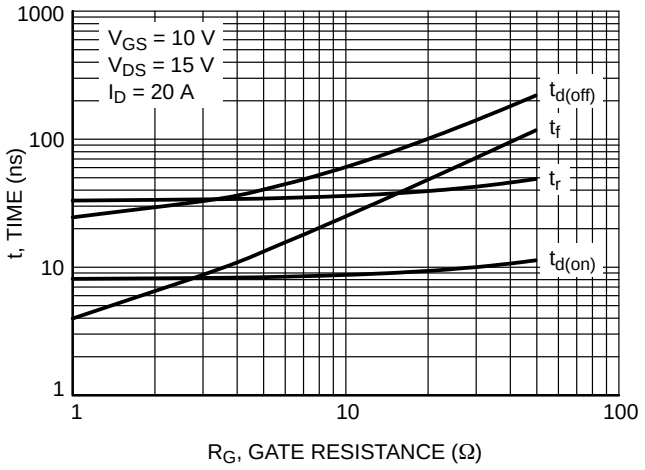


Figure 9. On−Region Characteristics

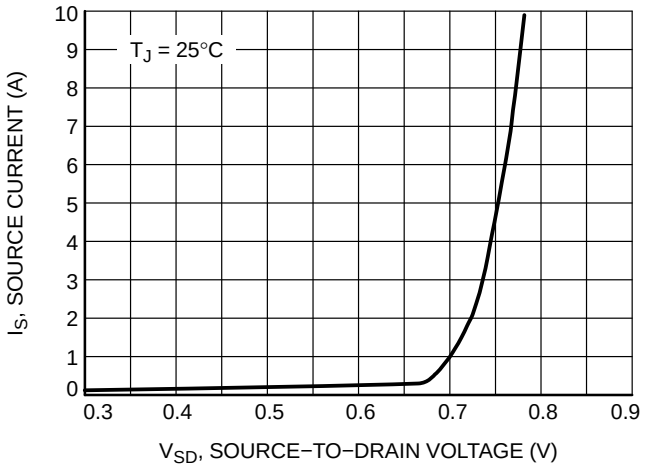


Figure 10. Diode Forward Voltage vs. Current

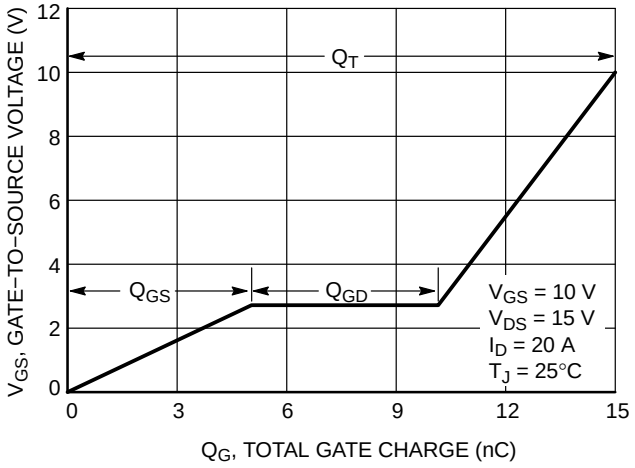


Figure 11. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

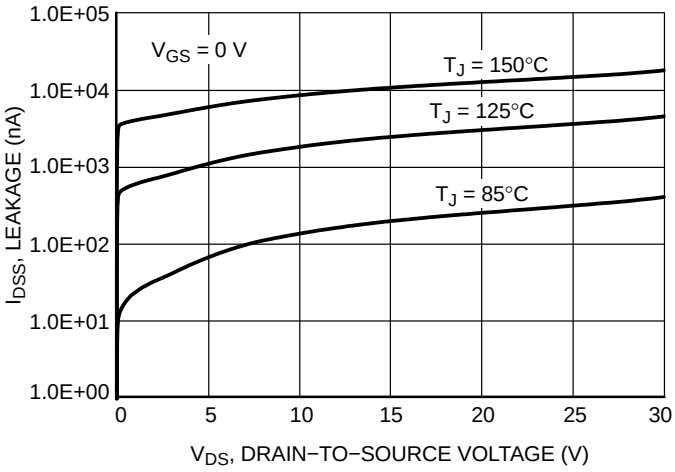


Figure 12. Drain−to−Source Leakage Current vs. Voltage

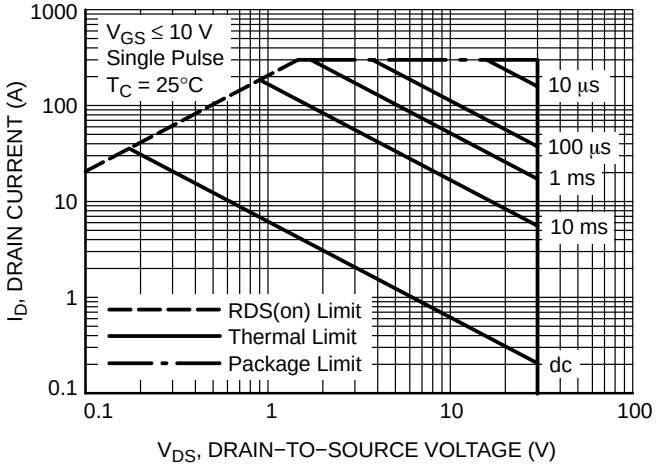


Figure 13. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS − Q1

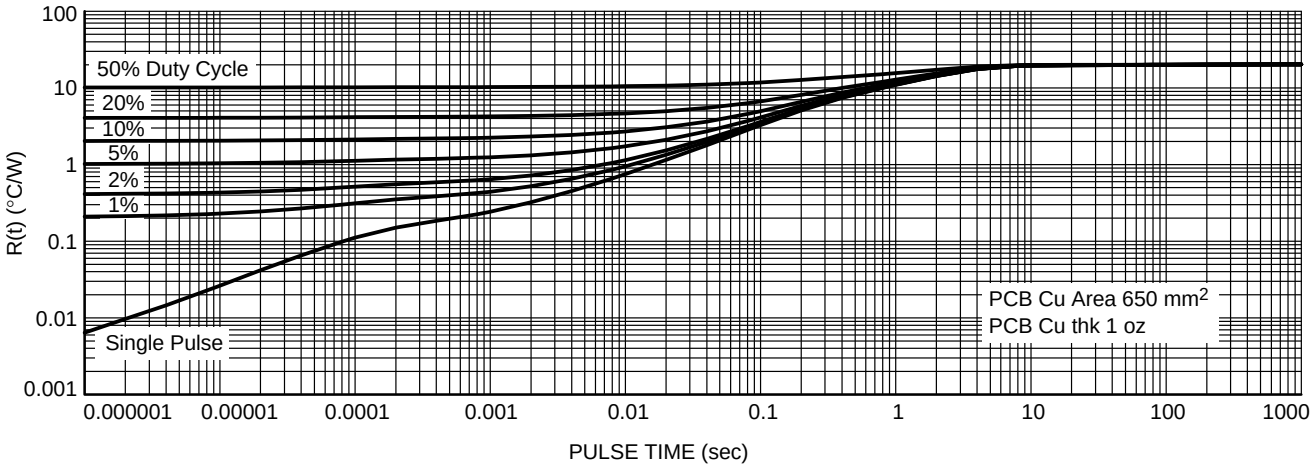


Figure 14. Thermal Characteristics

TYPICAL CHARACTERISTICS − Q2

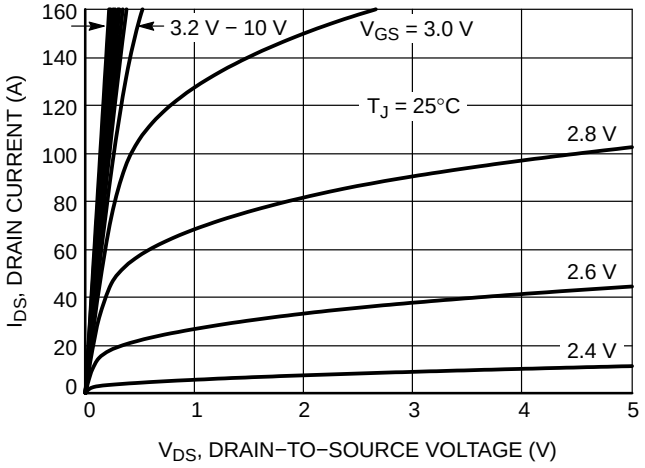


Figure 15. On−Region Characteristics

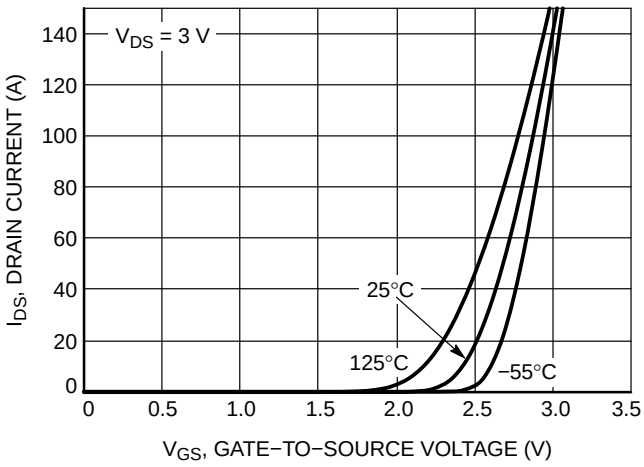


Figure 16. Transfer Characteristics

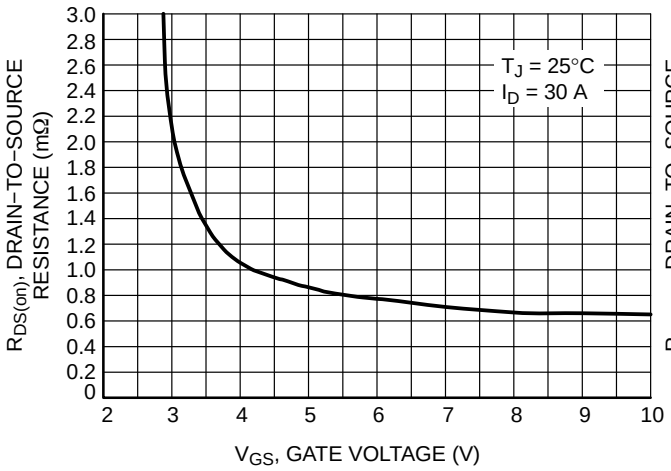


Figure 17. On−Resistance vs. Gate−to−Source Voltage

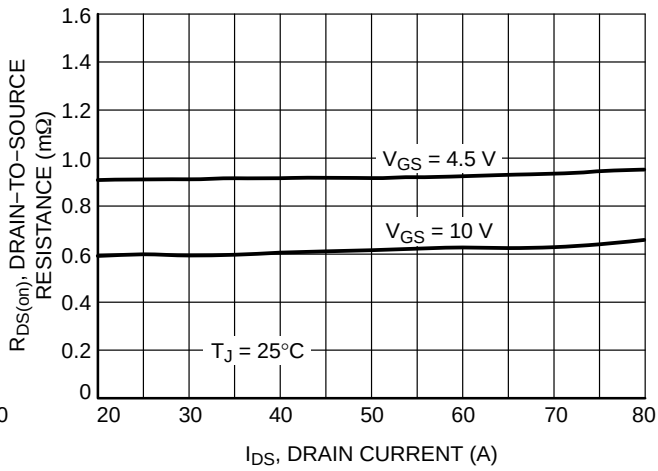


Figure 18. On−Resistance vs. Drain Current and Gate Voltage

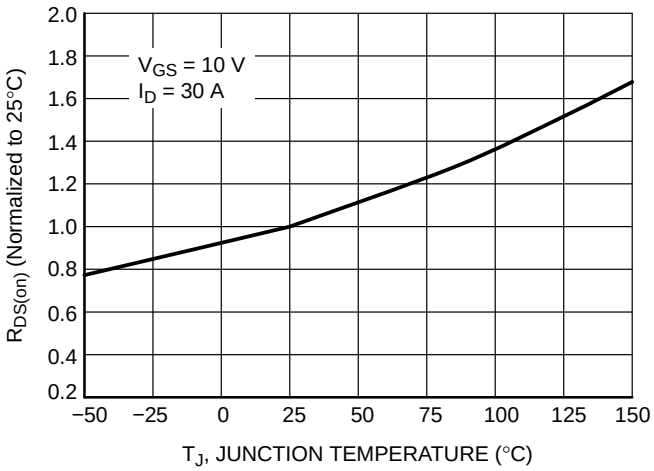


Figure 19. On−Resistance Variation with Temperature

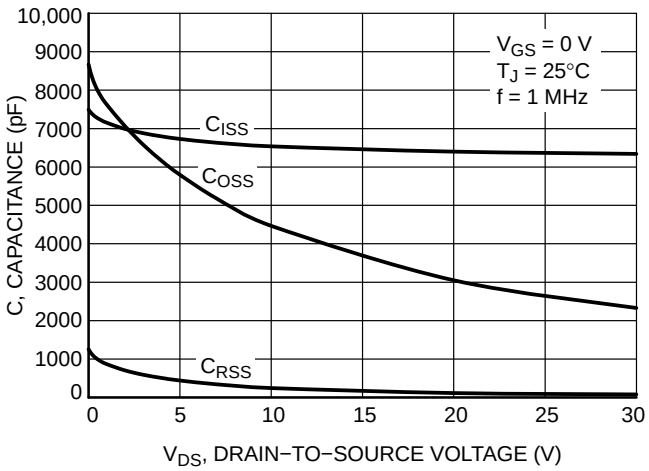


Figure 20. Capacitance Variation

TYPICAL CHARACTERISTICS − Q2

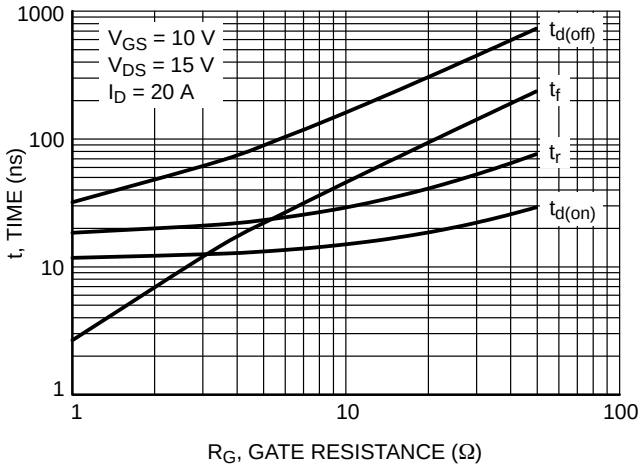


Figure 21. On−Region Characteristics

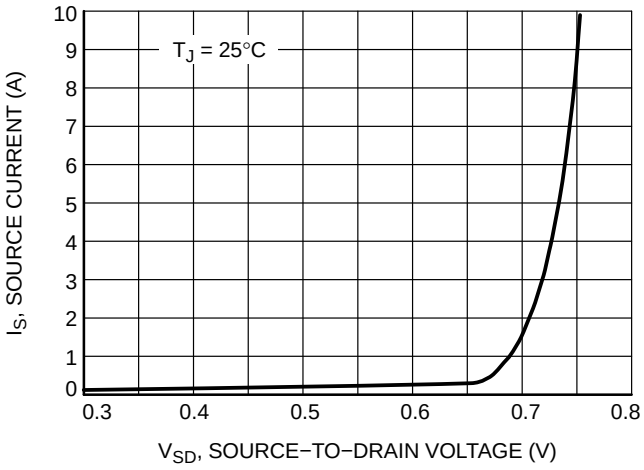


Figure 22. Diode Forward Voltage vs. Current

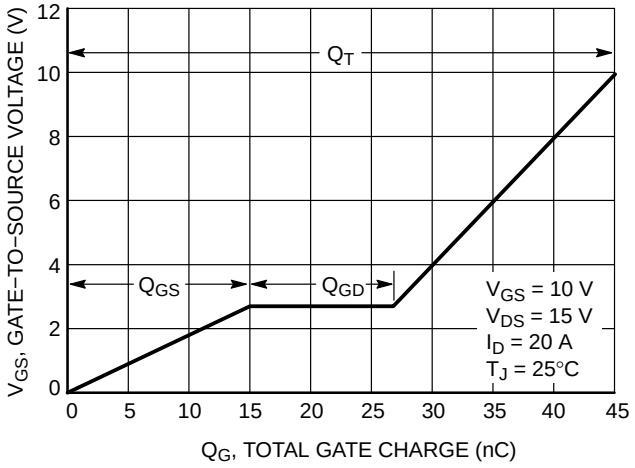


Figure 23. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

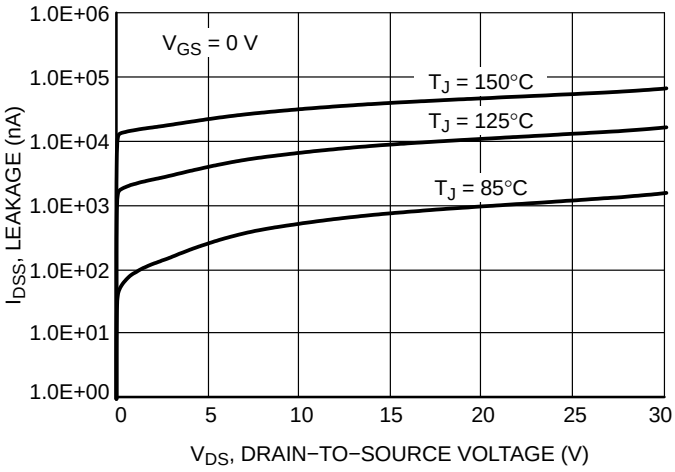


Figure 24. Drain−to−Source Leakage Current vs. Voltage

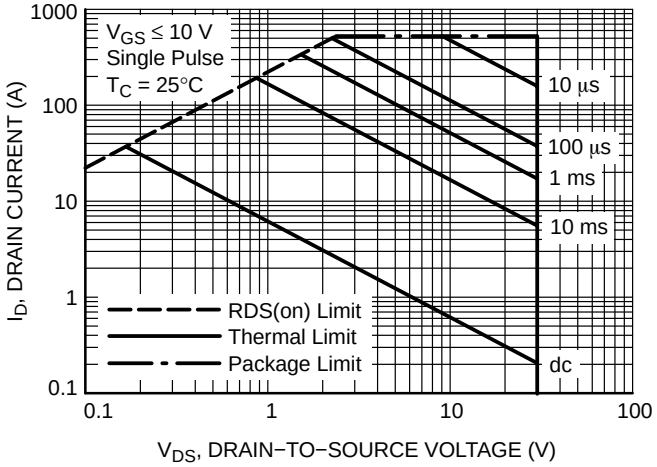


Figure 25. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS − Q2

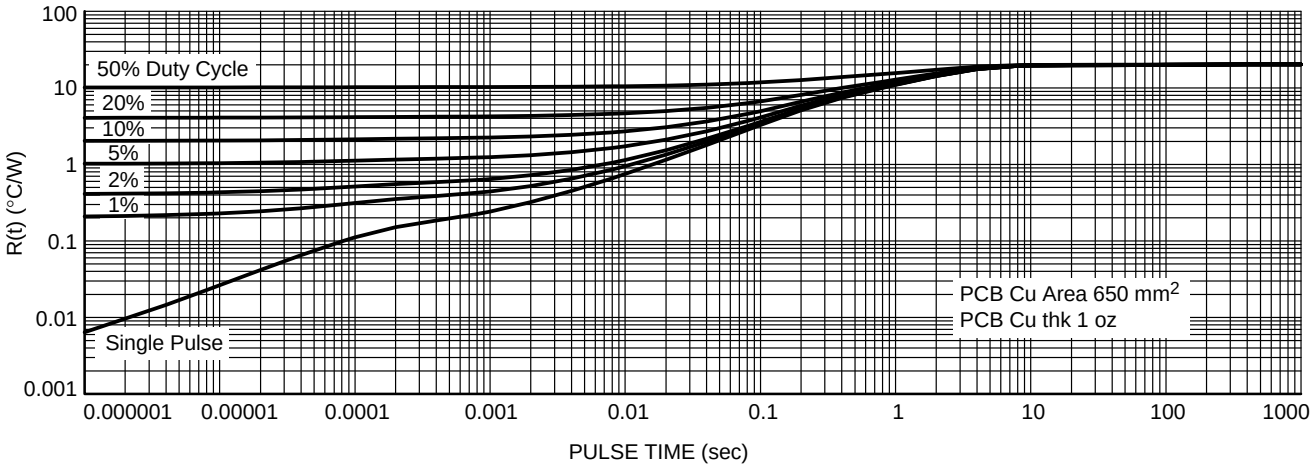


Figure 26. Thermal Characteristics

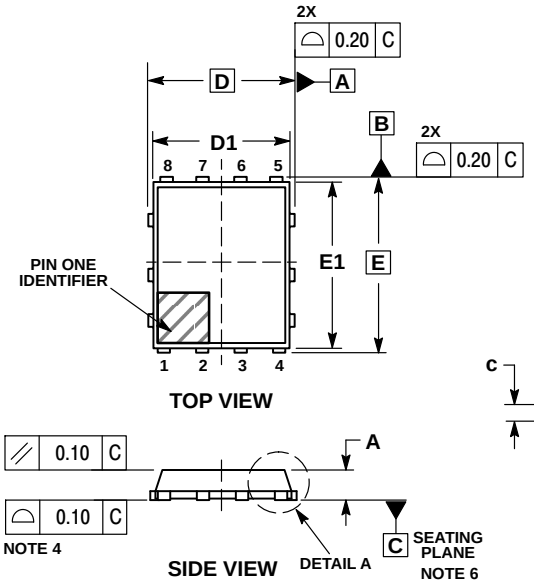
Ordering Information

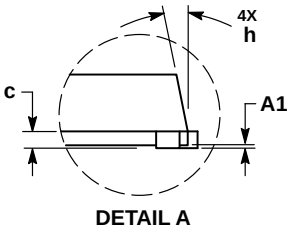
Device	Package	Shipping†
NTMFD4C85NT1G	DFN8 (Pb−Free)	1500 / Tape & Reel
NTMFD4C85NT3G	DFN8 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

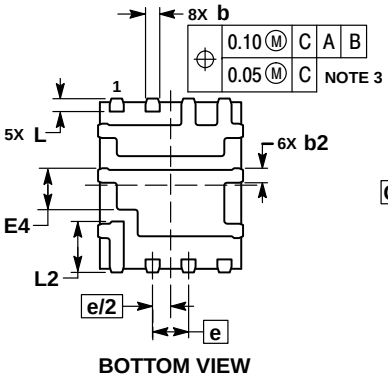
DFN8 5x6, 1.27P PowerPhase FET
CASE 506CR
ISSUE C

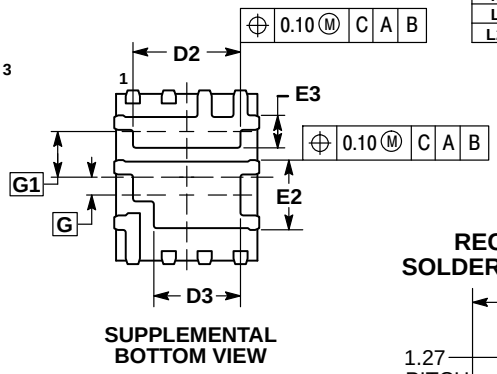




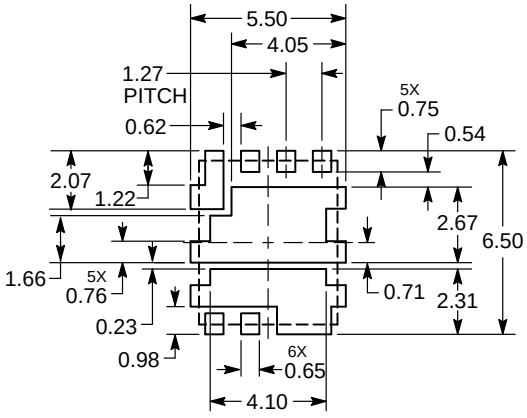
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b AND b1 APPLY TO PLATED TERMINAL AND ARE MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	0.90	1.10
A1	0.00	0.05
b	0.40	0.60
b2	0.40	0.60
c	0.20	0.30
D	5.15 BSC	
D1	4.90	5.10
D2	3.70	3.90
D3	2.96	3.16
E	6.15 BSC	
E1	5.80	6.00
E2	2.37	2.57
E3	1.05	1.25
E4	1.36	1.56
e	1.27 BSC	
G	0.625 BSC	
G1	1.615 BSC	
h	−−−	12 °
L	0.34	0.59
L2	1.68	1.93





RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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